METHOD OF ALTERING A BITSTREAM

ABSTRACT

A method is disclosed for redeploying an FPGA that has been restricted for use with a first design. The FPGA accepts only those configuration bitstreams whose CRC checksums match a value stored on the FPGA. The restricted FPGA is used with a second configuration bitstream for a second design by altering the second configuration bitstream so that it generates a CRC checksum that matches the value stored on the FPGA. The first checksum is derived by applying a CRC hash function to the first configuration bitstream. The second configuration bitstream is altered so that the second checksum generated when the CRC hash function is applied to the altered second configuration bitstream is identical to the first checksum. Altering the second configuration bitstream can result in an altered second configuration bitstream that is either longer than or the same length as the second configuration bitstream.